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EXAMINER	
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ART UNIT	PAPER NUMBER
2631	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,820	ZORTEA, ANTHONY EUGENE	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☒ Claim(s) *1-4,7,10,13,16,19,22 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

Reference number 100 (page 8 line 12)

FIG.1 reference numbers 270a-270d (page 11 line 22)

FIG. 6 reference number DFF 410 (page 15 line 8)

FIG. 6 reference number 415 (page 15 lines 9, 10, 11, 13, 14)

FIG. 6 reference number 420 (page 15 line 20)

FIG. 6 reference number 425a (page 15 line 22)

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

Page 8 line 12 block 100 is not shown in graphics.

Page 11 line 22 blocks 270a-270d are not shown in graphics.

Page 15 lines 8 block DFF 410 is not shown in graphics.

Page 15 lines 9, 10, 11, 13, and 14 block 415 are not shown in graphics.

Page 15 lines 20 block 420 is not shown in graphics.

Page 15 lines 22 block 425a is not shown in graphics.

Page 15 lines 31-32 the recitation "(Alternatively, a divider may be employed in lieu of the subtractor to produce a ratio instead of a difference.)" this may cause undesirable behavior in the case that the denominator in one of the comparators is zero will produce a very high value at the output (in theory infinite), and the rest of the comparisons will not be taken into account. It is suggested to delete this sentence or to modify in the way that this situation is taken into account.

Page 19 line 27 the recitation " 270" " is indefinite, it is suggested to be changed to " 270' ".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

The term "resolution" in claims 1-26 is a relative term which renders the claim indefinite. The term "resolution" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Applicant define

resolution in the disclosure as follows: "the resolution is a resolution between leading and trailing edges of the received signal" and "the resolution is a resolution between allowed amplitude levels of the received signal", so the applicant define "resolution" as a "resolution", so it is not clear what it is meant.

Claim Objections

Claims 1-4 are objected to because of the following informalities: in line 3 of claim 1 the recitation "near of the channel" is indefinite, it is suggested to be changed to "near end of a channel". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4-5, 8, 11, 14, 17, 20, 23 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Itri (US 5864592).

As per claim 1 Itri discloses a bi-directional communication having plural channels, each of said channels comprising: a master (Central Office) connected at a near end of a channel and a slave (Remote station) connected at an opposite end of channel (figure 5 central office station and remote station column 5 lines 53-54); the

master comprising: (a) a transmitter coupled to channel and having a master Tx clock signal (figure 5 block XMT CLK1 column 5 line 56); (b) receiver coupled to the channel and comprising (figure 5 RCV CLK1 column 5 line 60): i) an analog-to-digital converter that periodically samples at a sampling time Ts (figure 7 block 300 column 6 lines 38-41); ii) a clock recovery circuit that signal embedded generates a master Rx signal received from the channel (figure 5 block 232 column 5 lines12-15 and column 5 line 60); iii) a metric processor connected to an output of said analog-to-digital converter that produces a metric signal indicative of resolution of the received signal (figure 5 output oh RCV CLK1 phase error detector column 5 line 60); the slave comprising: (a) a receiver coupled to the channel and comprising a clock recovery circuit for generating a Slave Rx clock from the signal received from the master (figure 5 block RCV CLK3 and phase error detector out of RCV CLK3 column 5 line 59); (b) a transmitter coupled to the channel and having a Slave Tx clock signal, whereby said master Rx clock signal is frequency locked to said Slave Tx clock signal (figure 5 XMT CLK3 column 5 line 59); (c) a controllable delay element for generating said Slave Tx clock signal from said Slave Rx clock signal (figure 5 Phase adjust column 5 lines 15-24); the communication link further comprising a decision processor responsive to said metric processor for changing a delay value of said controllable delay element so as to maximize the metric signal (figure 5 blocks 206 and 240 column 6 lines 3-6).

As per claim 4 Itri discloses a second controllable delay between the Master Rx clock signal and the analog-to-digital converter and responsive to said decision processor, and the decision processor delays the Slave Tx clock signal and the sample

time Ts independently to maximize the metric signal (figure 6 block 246 column 6 lines 6-10).

As per claim 5 Itri discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, the bi-directional communication link (figure 5 column 5 lines 53-62); comprising: a metric processor for each master that produces a metric signal indicative of resolution of a signal received by the master from the corresponding slave (figure 5 block 240 column 6 lines 3-6); and a decision processor responsive to said metric processor for changing the phase of the Slave Tx clock relative to the Slave Rx clock so as to maximize the metric signal (figure 5 block 246 column 6 lines 6-11).

As per claim 8 Itri discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency locked to the Master Rx clock, said bi-directional communication link comprising (figure 7 column 6 lines 39-41 and lines 49-51) a metric processor for each master that produces a metric signal indicative of resolution of a signal received by the master from the corresponding slave (figure 5 block 240 column 6 lines 3-6); and a decision processor responsive to said metric processor for shifting

said sample time Ts relative to the Master Tx clock so as to maximize the metric signal (figure 5 block 246 column 6 lines 6-11).

As per claim 11 Itri discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock wherein each master receives a periodic noise burst comprising cross-talk (crosstalk is inherited in subscriber lines denoted as NEXT and FEXT crosstalk and it is described in "Understanding Subscriber Line Technology" T. Starr, J. Cioffi and P. Silverman ISBN 0-13-780545-4 Ed. 1999 Prentice Hall PTR pp 86- 92 also in "DSL simulation Techniques and Standards Development for Digital Subscriber line Systems" W. Chen ISBN 1-57870-017-7 Macmillan Technical Publishing 1998 pp 60-67) from masters of adjacent channels and echoes of itself (figure 2 block 56 column 3 line 46, figure 7 block 312), said noise capable of reducing the resolution of a signal received by the master from the slave over the corresponding communication, said bi-directional communication link comprising (figure 5 column 5 lines 53-62 and lines 49-51): a metric processor for each master that produces a metric signal indicative of the resolution of the signal received by the master from the corresponding slave (figure 5 block 240 column 6 lines 3-6); and a decision processor responsive to said metric processor for changing the phase of the Slave Tx clock relative to the Slave Rx clock so as to reduce the effects of the noise burst on the received signal and thereby increase the metric signal (figure 5 block 246 column 6 lines 6-11).

As per claim 14 Itri discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency (figure 7 block 300 column 6 line 39-41) locked to the Master Rx clock, and wherein each master receives a periodic noise burst comprising cross-talk (crosstalk is inherited in subscriber lines denoted as NEXT and FEXT crosstalk and it is described in "Understanding Subscriber Line Technology" T. Starr, J. Cioffi and P. Silverman ISBN 0-13-780545-4 Ed. 1999 Prentice Hall PTR pp 86-92 also in "DSL simulation Techniques and Standards Development for Digital Subscriber line Systems" W. Chen ISBN 1-57870-017-7 Macmillan Technical Publishing 1998 pp 60-67) from masters of adjacent channels and echoes (figure 2 block 56 column 3 line 46, figure 7 block 312) of itself said noise capable of reducing the resolution of a signal received by the master from the slave over the corresponding communication, said bi-directional communication link comprising: a metric processor for each master that produces a metric signal indicative of the resolution of the signal received by the master from the corresponding slave (figure 5 block 240 column 6 lines 3-6); and a decision processor responsive said for shifting said sample time Ts relative the Tx clock so as to reduce the effects of the noise and thereby increase the metric (figure 5 block 246 column 6 lines 6-11).

As per claim 17 Itri discloses a controllable delay between the Slave Rx clock and the Slave Tx clock, said decision processor governing said controllable delay so as the shift said sample time Ts (figure 5 block 246 column 5 lines 48-52).

As per claim 20 Itri discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clockr and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency (figure 7 block 300 column 6 line 39-41) locked to the Master Rx clock, and wherein each master receives a periodic noise burst comprising cross-talk (crosstalk is inherited in subscriber lines denoted as NEXT and FEXT crosstalk and it is described in "Understanding Subscriber Line Technology" T. Starr, J. Cioffi and P. Silverman ISBN 0-13-780545-4 Ed. 1999 Prentice Hall PTR pp 86-92 also in "DSL simulation Techniques and Standards Development for Digital Subscriber line Systems" W. Chen ISBN 1-57870-017-7 Macmillan Technical Publishing 1998 pp 60-67) from masters of adjacent channels and echoes of itself (figure 2 block 56 column 3 line 46, figure 7 block 312), said noise capable of reducing the resolution of a signal received by the master from the slave over the corresponding communication, a method of reducing the effects of the cross-talk and echo noise burst on the signal received by each master, comprising: for each master, producing a metric signal indicative of the resolution of the signal received by the master from the corresponding slave (figure 5 block 240 column 6 lines 3-6); and in response to said metric signal, shifting said sample time Ts relative

to the Master Tx clock so as to reduce the effects of the noise burst on the received signal and thereby increase the metric signal (figure 5 block 246 column 6 lines 6-11).

As per claim 23 Itri discloses a controllable delay between the Slave Rx clock and the Slave Tx clock, said decision processor governing said controllable delay so as the shift said sample time Ts (figure 5 block 246 column 5 lines 48-52).

As per claim 26 Itri discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts (figure 7 block 300 column 6 line 39-41) frequency locked to the Master Rx clock, and wherein each master receives a periodic noise burst comprising cross-talk (crosstalk is inherited in subscriber lines denoted as NEXT and FEXT crosstalk and it is described in "Understanding Subscriber Line Technology" T. Starr, J. Cioffi and P. Silverman ISBN 0-13-780545-4 Ed. 1999 Prentice Hall PTR pp 86-92 also in "DSL simulation Techniques and Standards Development for Digital Subscriber line Systems" W. Chen ISBN 1-57870-017-7 Macmillan Technical Publishing 1998 pp 60-67) from masters of adjacent channels and echoes of itself (figure 2 block 56 column 3 line 46, figure 7 block 312), said noise capable of reducing the resolution of a signal received by the master from the slave over the corresponding communications a method of reducing the effects of the cross-talk and echo noise burst on the signal received by each master, comprising: for each master, producing a metric signal indicative of the resolution of the

signal received by the master from the corresponding slave(figure 5 block 240 column 5 lines 45-52); for each slave, producing a metric signal indicative of the resolution of the signal received by the slave from the corresponding master (figure 5 block 206 column 5 lines 28-34); and in response to the metric signal corresponding to the master and to the metric signal corresponding to the slave, shifting said sample time Ts relative to the Master Tx clock so as to reduce the effects of the noise (figure 5 block 218 column 5 lines 35-44)

Claims 1, 5 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Rakib (US 6307868).

As per claim 1 Rakib discloses a bi-directional communication having plural channels, each of said channels comprising: a master connected at a near end of a channel and a slave connected at an opposite end of channel (figure 1 central unit and remote unit column 4 lines 8-20); the master comprising: (a) a transmitter coupled to channel and having a master Tx clock signal (figure 1 block 24 column 4 line 11); (b) receiver coupled to the channel and comprising (figure 1 block 70 column 4 lines 29-30): i) an analog-to-digital converter that periodically samples at a sampling time Ts (the ADC is inherit in the receiver of a data communications, because the signal is received as an analog signal and it has to be converted to digital values); ii) a clock recovery circuit that signal embedded generates a master Rx signal received from the channel (figure 1 block 32 column 4 lines 34-35); iii) a metric processor connected to an output of said analog-to-digital converter that produces a metric signal indicative of resolution of the received signal (figure 1 lateral input block 32 column 4 lines 8-20); the slave

comprising: (a) a receiver coupled to the channel and comprising a clock recovery circuit for generating a Slave Rx clock from the signal received from the master (figure 1 lateral input block 34 column 4 lines 15); (b) a transmitter coupled to the channel and having a Slave Tx clock signal, whereby said master Rx clock signal is frequency locked to said Slave Tx clock signal (figure 1 lateral input block 6 column 4 lines 24); (c) a controllable delay element for generating said Slave Tx clock signal from said Slave Rx clock signal (figure 1 lateral input block 42 column 4 lines 15-24); the communication link further comprising a decision processor responsive to said metric processor for changing a delay value of said controllable delay element so as to maximize the metric signal (figure 6 column 22 lines 8-26).

As per claim 5 Rakib discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, the bi-directional communication link (figure 1 block 32 column 4 lines 11-40); comprising: a metric processor for each master that produces a metric signal indicative of resolution of a signal received by the master from the corresponding slave (figure 1 block 32 column 4 lines 29-36); and a decision processor responsive to said metric processor for changing the phase of the Slave Tx clock relative to the Slave Rx clock so as to maximize the metric signal (figure 1 block 76 column 4 lines 36-38).

As per claim 8 Rakib discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels,

each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency locked to the Master Rx clock, said bi-directional communication link comprising (figure 1 block 32 column 4 lines 11-40) a metric processor for each master that produces a metric signal indicative of resolution of a signal received by the master from the corresponding slave (figure 1 block 32 column 4 lines 29-36); and a decision processor responsive to said metric processor for shifting said sample time Ts relative to the Master Tx clock so as to maximize the metric signal (figure 1 block 76 column 4 lines 36-38).

Claims 1, 2, 4-6, 8, 9, 11, 12, 14, 15, 17, 18, 20, 21, 23, 24 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Trans (US 6377640).

As per claim 1 Trans discloses a bi-directional communication having plural channels, each of said channels comprising: a master connected at a near end of a channel and a slave connected at an opposite end of channel (figures 8-1, 8-2 and 8A column 14 lines 1-7); the master comprising: (a) a transmitter coupled to channel and having a master Tx clock signal (figure 3 transmitter section figure 10 column 14 line 10); (b) receiver coupled to the channel and comprising (figure 3 receiver section figure 10 column 14 line 10): i) an analog-to-digital converter that periodically samples at a sampling time Ts (figure 3 analog section 34 and digital section 32 figure 34 block 22 column 59 line 51); ii) a clock recovery circuit that signal embedded generates a master Rx signal received from the channel (figure 3 block 355, figure 8A block 311 column 14

line 30); iii) a metric processor connected to an output of said analog-to-digital converter that produces a metric signal indicative of resolution of the received signal (figure 8-2 block 144 column 17 lines 41-48); the slave comprising: (a) a receiver coupled to the channel and comprising a clock recovery circuit for generating a Slave Rx clock from the signal received from the master (figure 3 receiver section figure 10 column 14 line 10); (b) a transmitter coupled to the channel and having a Slave Tx clock signal, whereby said master Rx clock signal is frequency locked to said Slave Tx clock signal (figure 3 transmitter section figure 10 column 14 line 10); (c) a controllable delay element for generating said Slave Tx clock signal from said Slave Rx clock signal (figure 34 column 64 line 32); the communication link further comprising a decision processor responsive to said metric processor for changing a delay value of said controllable delay element so as to maximize the metric signal (figure 5a block M212 column 16 lines 37-38).

As per claims 2, 6, 9, 12, 15, 18, 21 and 24 Trans discloses that the resolution is between leading and trailing edges of the received signal using eye patterns (figures 6C, 6D, 24 and 27 column 36 line 5).

As per claim 4 Trans discloses a second controllable delay between the Master Rx clock signal and the analog-to-digital converter and responsive to said decision processor, and the decision processor delays the Slave Tx clock signal and the sample time Ts independently to maximize the metric signal (figure 5a column 34 lines 24-28).

As per claim 5 Trans discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels,

each master issuing a Master Tx clock each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, the bi-directional communication link (figures 8-1, 8-2, 8A and 10C-2 column 14 lines 1-7); comprising: a metric processor for each master that produces a metric signal indicative of resolution of a signal received by the master from the corresponding slave (figure 8-2 block 144 column 17 lines 41-48); and a decision processor responsive to said metric processor for changing the phase of the Slave Tx clock relative to the Slave Rx clock so as to maximize the metric signal (figure 5a block M212 column 16 lines 37-38).

As per claim 8 Trans discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency locked to the Master Rx clock, said bi-directional communication link comprising (figures 8-1, 8-2, 8A and 10C-2 column 14 lines 1-7) a metric processor for each master that produces a metric signal indicative of resolution of a signal received by the master from the corresponding slave (figure 8-2 block 144 column 17 lines 41-48); and a decision processor responsive to said metric processor for shifting said sample time Ts relative to the Master Tx clock so as to maximize the metric signal (figure 5a column 34 lines 24-28).

As per claim 11 Trans discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock wherein each master receives a periodic noise burst comprising cross-talk (figures 1B-1 1B-2, 1B-3, 5b and 5d column 35 line 47) from masters of adjacent channels and echoes of itself, said noise capable of reducing the resolution of a signal received by the master from the slave over the corresponding communication, said bi-directional communication link comprising: a metric processor for each master that produces a metric signal indicative of the resolution of the signal received by the master from the corresponding slave (figure 8-2 block 144 column 17 lines 41-48); and a decision processor responsive to said metric processor for changing the phase of the Slave Tx clock relative to the Slave Rx clock so as to reduce the effects of the noise burst on the received signal and thereby increase the metric signal (figure 5a column 34 lines 24-28).

As per claim 14 Trans discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency locked to the Master Rx clock, and wherein each master receives a periodic noise burst comprising cross-talk (figures 1B-1 1B-2, 1B-3, 5b and

5d column 35 line 47) from masters of adjacent channels and echoes (figure 10C-2) of itself said noise capable of reducing the resolution of a signal received by the master from the slave over the corresponding communication, said bi-directional communication link comprising: a metric processor for each master that produces a metric signal indicative of the resolution of the signal received by the master from the corresponding slave (figure 8-2 block 144 column 17 lines 41-48); and a decision processor responsive said for shifting said sample time Ts relative the Tx clock so as to reduce the effects of the noise and thereby increase the metric (figure 5a column 34 lines 24-28).

As per claim 17 Trans discloses a controllable delay between the Slave Rx clock and the Slave Tx clock, said decision processor governing said controllable delay so as the shift said sample time Ts (figure 5a column 34 lines 24-28).

As per claim 20 Trans (US 6377640) discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency (figure 5a column 34 lines 24-28) locked to the Master Rx clock, and wherein each master receives a periodic noise burst comprising cross-talk (figures 1B-1 1B-2, 1B-3, 5b and 5d column 35 line 47) from masters of adjacent channels and echoes of itself (figure 10C-3), said noise capable of reducing the resolution of a signal received by the master from the slave over the

corresponding communication, a method of reducing the effects of the cross-talk and echo noise burst on the signal received by each master, comprising: for each master, producing a metric signal indicative of the resolution of the signal received by the master from the corresponding slave (figure 8-2 block 144 column 17 lines 41-48); and in response to said metric signal, shifting said sample time Ts relative to the Master Tx clock so as to reduce the effects of the noise burst on the received signal and thereby increase the metric signal (figure 5a column 34 lines 24-28).

As per claim 23 Trans discloses a controllable delay between the Slave Rx clock and the Slave Tx clock, said decision processor governing said controllable delay so as the shift said sample time Ts (figure 5a column 34 lines 24-28).

As per claim 26 Trans discloses a bi-directional communication link having plural channels with respective masters and slaves at respective ends of respective channels, each master issuing a Master Tx clock, each slave constructing a Slave Rx clock frequency-locked to the Master Tx clock, and a Slave Tx clock frequency-locked to the Slave Rx clock, wherein the master samples a signal it receives from the slave at a sample time Ts frequency locked to the Master Rx clock, and wherein each master receives a periodic noise burst comprising cross-talk (figures 1B-1 1B-2, 1B-3, 5b and 5d column 35 line 47) from masters of adjacent channels and echoes of itself (figure 10C-3), said noise capable of reducing the resolution of a signal received by the master from the slave over the corresponding communications a method of reducing the effects of the cross-talk and echo noise burst on the signal received by each master, comprising: for each master, producing a metric signal indicative of the resolution of the

signal received by the master from the corresponding slave(figure 8-2 block 144 column 17 lines 41-48); for each slave, producing a metric signal indicative of the resolution of the signal received by the slave from the corresponding master (figure 8-2 block 144 column 17 lines 41-48); and in response to the metric signal corresponding to the master and to the metric signal corresponding to the slave, shifting said sample time Ts relative to the Master Tx clock so as to reduce the effects of the noise (figure 8-2 block 15)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 6, 9, 12, 15 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itri (US 5864592) as applied to claims 1, 5, 8, 11, 14 and 20 above, and further in view of Klemmer (US 6265902). Itri discloses claims 1, 5, 8, 11, 14 and 20, Itri doesn't disclose that the resolution is between leading and trailing edges of the received signal. Klemmer discloses a digital phase detector where the resolution is between leading and trailing edges of the received signal (column 2 lines 8-9). Itri and Klemmer disclosures are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the digital phase detector disclosed by Klemmer in the communication system disclosed by Itri. The suggestion/motivation for doing so

would have been to reduce the phase-lock loop lock time (Klemmer column 1 line 8) and to increase the stability of the received signal by the master unit. Therefore, it would have been obvious to combine Itri and Klemmer to obtain the invention as specified in claims 2, 6, 9, 12, 15 and 21.

Claims 2, 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rakib (US 6307868) as applied to claims 1, 5 and 8 above, and further in view of Klemmer (US 6265902). Rakib discloses claims 1, 5 and 8, Rakib doesn't disclose that the resolution is between leading and trailing edges of the received signal. Klemmer discloses a digital phase detector where the resolution is between leading and trailing edges of the received signal (column 2 lines 8-9). Rakib and Klemmer disclosures are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the digital phase detector disclosed by Klemmer in the communication system disclosed by Rakib. The suggestion/motivation for doing so would have been to reduce the phase-lock loop lock time (Klemmer column 1 line 8) and to increase the stability of the received signal by the master unit. Therefore, it would have been obvious to combine Rakib and Klemmer to obtain the invention as specified in claims 2, 6 and 9.

Claims 18 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itri (US 5864592), further in view of Klemmer (US 6265902), and further in view of Chang (US 6316966).

As per claim 18 Itri and Klemmer teach claim 15. Itri and Klemmer don't teach that the metric processor comprises a processor for computing an opening in an eye

diagram of the signal received by the master. Chang discloses that the eye diagram is used to control a phase detector (figure 6 column 9 line 20-26). Itri, Klemmer and Chang disclosures are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the eye diagram disclosed by Chang with the system disclosed by Itri and Klemmer. The suggestion/motivation for doing so would have been to establishing a late clock boundary condition and an early clock boundary condition (Chang figure 6 column 9 line 20-26). Therefore, it would have been obvious to combine Itri, Klemmer and Chang to obtain the invention as specified in claim 18.

As per claim 24 Itri and Klemmer teach claim 21. Itri and Klemmer don't teach that the metric processor comprises a processor for computing an opening in an eye diagram of the signal received by the master. Chang discloses that the eye diagram is used to control a phase detector (figure 6 column 9 line 20-26). Itri, Klemmer and Chang disclosures are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the eye diagram disclosed by Chang with the system disclosed by Itri and Klemmer. The suggestion/motivation for doing so would have been to establishing a late clock boundary condition and an early clock boundary condition (Chang figure 6 column 9 line 20-26). Therefore, it would have been obvious to combine Itri, Klemmer and Chang to obtain the invention as specified in claim 24.

Claims 18 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itri (US 5864592), further in view of Klemmer (US 6265902), and further in view of Hogge (US 4218771).

As per claim 18 Itri and Klemmer teach claim 15. Itri and Klemmer don't teach that the metric processor comprises a processor for computing an opening in an eye diagram of the signal received by the master. Hogge discloses that the eye diagram is used to control a phase detector (column 2 lines 51-53). Itri, Klemmer and Hogge disclosures are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the eye diagram disclosed by Hogge with the system disclosed by Itri and Klemmer. The suggestion/motivation for doing so would have been to establishing a late clock boundary condition and an early clock boundary condition (Hogge column 2 lines 51-53). Therefore, it would have been obvious to combine Itri, Klemmer and Hogge and Chang to obtain the invention as specified in claim 18.

As per claim 24 Itri and Klemmer teach claim 21. Itri and Klemmer don't teach that the metric processor comprises a processor for computing an opening in an eye diagram of the signal received by the master. Hogge discloses that the eye diagram is used to control a phase detector (column 2 lines 51-53). Itri, Klemmer and Hogge disclosures are analogous art because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the eye diagram disclosed by Hogge with the system disclosed by Itri and Klemmer. The suggestion/motivation for doing so would have been to establishing a

late clock boundary condition and an early clock boundary condition (Hogge column 2 lines 51-53). Therefore, it would have been obvious to combine Itri, Klemmer and Hogge and Chang to obtain the invention as specified in claim 24.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAT 11-29-2004

M. G

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER